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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/966,391	09/28/2001	Paul W. DeMone	MOSA-01001US1	6511

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EXAMINER	
NGUYEN, MINH T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 02/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/966,391	DEMONE, PAUL W.	
	Examiner	Art Unit	
	Minh Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-28 and 30-35* is/are rejected.

7)☒ Claim(s) *29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 November 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/30/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 11/30/04 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 21-28 and 30-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,483,434, issued to Seesink in view of Kazerounian (EU Publication No. 323,156, publication date 7/5/1989).

As per claim 21, Seesink discloses a charge pump (Fig. 1A) for a DRAM (this is merely an intended use of a charge pump circuit having the structure discussed below), comprising:

a first (D10, ..., D1(N-1), C11, ..., C1N) and second (D20, ..., D2(N-1), C21, ..., C2N) pump cascades coupled in parallel (they are in parallel between nodes VDD and HVOUT) to an output node (HVOUT), each pump cascade having a plurality of pump stages coupled in series (first: D10, ..., D1(N-1) are in series, and second: D20, ..., D2(N-1) are in series), the output node receiving the charge pumped by the first and second pump cascades (they are both connected to output node HVOUT) and providing the output supply voltage that is greater in magnitude than a power supply voltage (this is the function of any charge pump circuit); and

each pump stage has a diode and a capacitor (as shown).

Seesink does not explicitly disclose FETs are used to implement diode and capacitor in each of the pump stage and the FETs of the last pump stage of each cascade having an oxide thickness greater than the FETs of the first pump stage of each cascade as called for in the claim.

Kazerounian explicitly discloses that diodes and capacitors in each stage of a charge pump circuit can be implemented using FETs (for example, shown in Fig. 1, FET 14-1 is implemented to function as a diode, and in column 3, lines 1-6, FET is implemented to function as a capacitor). In fact, it is extremely popular to implement diodes and capacitors using FETs in an IC LSI. The advantage of configuring transistors functioned as diodes and capacitors are so well-known that it is even taught in elementary IC electronics textbooks which is to simplify the fabrication process and reduce the sizes of the diodes and capacitors.

Kazerounian further explicitly discloses that in a charge pump circuit, the further the stage from the input node, the higher the voltage pressured to the stage (column 1,

lines 31-38). Therefore, FETs used to implement the charge pump must withstand a high voltage to avoid broke down (column 1, lines 46-50). The well-known solution would be to fabricate all the FETs with thick gate oxides. Alternately, the other solution would be to fabricate FETs in stages which withstands low voltages with thin gate oxide and fabricate FETs in stages which must withstand high voltages with thick gate oxide (column 2, lines 10-21). He further discusses the advantages and disadvantages of each solution in that section.

It would have been obvious to one skilled in the art at the time of the invention was made to implement the Seesink's charge pump using FETs as taught in Kazerounian's reference wherein FETs of the last pump stage of each cascade having an oxide thickness greater than the FETs of the first pump stage of each cascade. The motivation and/or advantage would be to reduce the estate of the IC LSI and increase the operating speed of the charge pump as explicitly discussed in column 2, lines 10-21 of the Kazerounian's reference.

As per claim 22, the recited limitations are clearly shown in Fig. 1A of Seesink, i.e., first clock signal (phi1) and second clock signal (phi2).

As per claim 23, the combination discussed above does not disclose the FETs are PFETs as called for in the claim.

However, Kazerounian's reference explicitly teaches the advantage of using PFETs which is further enhancing the breakdown voltage (column 2, lines 43-55).

It would have been obvious to one skilled in the art at the time of the invention was made to implement the FETs using PFETs for the advantage discussed herein above.

As per claim 24, the recited limitation is shown in Fig. 1A of Seesink, i.e., the power supply voltage VDD is connected to the first pump stages.

As per claim 25, the recited coupling diodes read on diodes D1N and D2N.

As per claim 26, this claim is rejected for the same reasons and motivation discussed in claim 21.

As per claim 27, the recited limitation is disclosed in column 3, lines 32-35 of the Seesink's reference.

As per claim 28, the recited system clock is the clock generated by the oscillator 3 and because phi(1) and phi(2) are complement, charges to the output node responsive to both the rising and falling edges of the system clock.

As per claim 30, this claim is rejected for the same reasons and motivation discussed in claims 21 and 24.

As per claims 31-34, the claims are rejected for the same reasons as claims 22-23, 26 and 27, respectively.

As per claim 35, this claim is merely a method to operate a charge pump having a structure discussed in claim 21. Since the structure is disclosed, the method to operate such a structure is seen as obvious.

Allowable Subject Matter

3. Claim 29 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 29 is allowable because the prior art of record fails to disclose or suggest the inclusion of a latch, driving stages and equalization stage in the clock signal generator as recited in the claim.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is 571-272-1748. The examiner can normally be reached on Monday, Tuesday, Thursday, Friday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

2/4/05

Minh Nguyen
Primary Examiner
Art Unit 2816